INDIUM PHOSPHIDE FOR HIGH FREQUENCY POWER TRANSISTORS

V. L. Wrick, W. J. Choyke and R. C. Clarke

Final Report
For Period 22 March 1979 to 28 April 1980

28 September 1980

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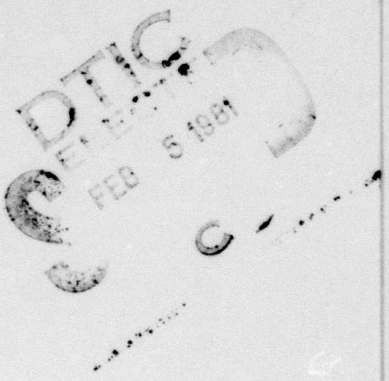

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This report covers the conclusion of studies aimed at determining the utility of InP for fabricating power microwave field effect transistors(FET's). This phase of the work provided working transistors which were modeled and compared to their GaAs counterparts.

Vapor phase epitaxy (VPE) results are provided for device structures which include high resistivity buffer layers. Ion implantation was aimed at a novel amorphization and low temperature regrowth study to provide implanted p-n junctions in InP for future JFET structures.

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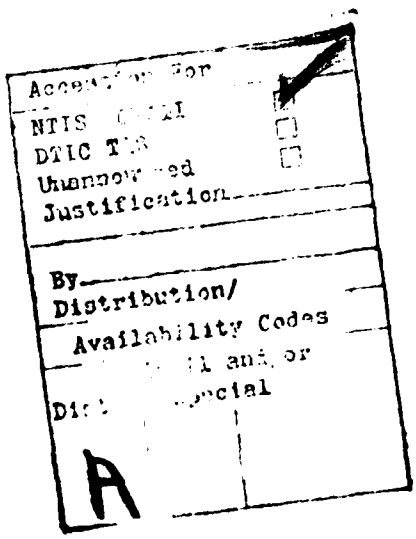
Processing technology concentrated on a self-aligned diffused gate JFET structure. This technique produced working microwave transistors (JFET) up to 1200 μm in gate periphery. The report compares these devices to similar GaAs transistors (MESFET) and makes recommendations for future studies.



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1. INTRODUCTION

The objective of this program has been to determine the utility of InP for producing power microwave field effect transistors (FET's). InP was originally considered as an alternative to GaAs because of several material parameters which theoretically offered improved device performance. Table 1-1 lists the key parameters and how one would expect them to impact FET operation. InP has been investigated in the past; hence, some of its drawbacks are also documented. Table 1-2 reviews the technological and theoretical problems associated with InP power FET's. The previous interim report reviewed the progress in achieving the technological goals of the program.
This report discusses the concluding effort which filled in the gaps in the InP FET technology base. The resulting transistors were extensively tested and modeled in an attempt to address the larger theoretical question of InP's place as an FET material.

The major technological problem with InP has been the low Schottky barrier height of metals on n-type InP. The previous report has detailed the Westinghouse studies on dielectric enhanced barriers. In light of these studies, it was determined that a p-n junction should provide the most reliable gating technique on InP. In the long term, ion implantation was deemed the best approach to achieving shallow, degenerate p-type doping for 1 μm gate lengths. Ion implantation, however, requires further development to consistently deliver these results. Therefore, preliminary work was begun on improving the p-type implant technology base, and simultaneously, a self-aligned diffused junction transistor was fabricated. This "demonstration vehicle" was then microwave tested and modeled to allow the opportunity for an analysis of device behavior.

This report represents the conclusion of the effort to investigate power InP FET's. Over the course of the program, reliable InP vapor phase epitaxy (VPE) and ion implantation were developed to support the device investigation. Amorphization and low temperature recrystallization of ^{31}P implants in InP were observed. A broad spectrum of gate technologies were addressed and a reasonable demonstration technique was achieved. Finally, rf modeling of the devices allowed a semi-quantitative comparison between the InP JFET and its counterpart, the GaAs MESFET. Recommendations for further study are included in the final section of the report.

Table 1-1

Technological Problems with the InP FET

A. Reproducible, High Mobility VPE Layers Suitable for FET Fabrication

B. Develop Low Leakage Schottky Gate

C. Develop P-N Junction Gate

   a. Ion Implantation

   b. Diffused Junction

Table 1-2

Theoretical Questions Regarding the Viability of the InP Power FET

A. Determine the Nature and Behavior of the Gate-Drain Feedback Capacitance

B. Determine Device Design Parameters (Gate Length, Gate-Drain Spacing, Doping, Gate Recess) Which Differ from GaAs Technology in Affecting the Power and Frequency Limitations of the Device

2. VAPOR PHASE EPITAXY

2.1 Introduction

The $PC\ell_3|In|H_2$ or chloride process for the growth of indium phosphide epitaxial layers has been in use for many years. A carefully controlled concentration of phosphorus trichloride vapor in hydrogen is passed over indium at high temperatures (700-750°C) and the products, indium monochloride and phosphorus vapor, pass over polished seed wafers at 650°C. Epitaxy of indium phosphide subsequently takes place on the seed wafer with a growth rate and impurity content dependent on the purity of the raw materials and, more importantly, on the growth conditions employed. The mole fraction of phosphorus trichloride, the gas phase stoichiometry, and the source and seed temperature distribution profiles are the most significant variables in the process.

For electronic devices a thin layer of semiconductor is grown on the surface of an indium phosphide seed wafer and, as the layer propagates away from the substrate, impurities are deliberately added to modify the crystal so as to produce a controlled profile of electron concentration with depth, frequently with submicron dimensions. Our previous report (243-023-T1, Annual Technical Report, September 1979) discussed the reactor design for epitaxy of InP, morphology control, multilayer growth and wafer characterization. At that time, however, a problem with the appearance of a low mobility conducting region at the interface between the iron doped substrates and the buffer layers occurred. This layer has now been eliminated.

2.2 Growth Transients

The interface layer was traced to the growth transients during the heating of the epitaxial system. Since all the indium phosphide

that dissolved in the indium melt has precipitated during cool-down, in reheating the melt the solid must dissolve again. Using a furnace with a heat pipe to promote an even temperature over the source, and using an initial heating cycle designed to prevent seed decomposition, the epitaxial deposition can begin with the passage of PCl_3 vapor over the source. However, a transient occurs at the moment of the arrival of the PCl_3 at the source. Phosphorus formed by the decomposition of PCl_3 in hydrogen dissolves in the exposed indium melt to cover the same with a skin of indium phosphide. The length of the transient is a function of the rate of arrival of phosphorus vapor and the source dimensions and temperature gradient. This phenomenon is significant because it embodies a changing gas phase stoichiometry over the seeds. At first the phosphorus pressure over the seeds is determined by the indium phosphide decomposition at the source but as the skin area becomes a greater fraction of the total, phosphorus begins to flow past the source. Thus, we can expect a gradually increasing phosphorus to indium ratio until the steady state is reached. Ten to fifteen minutes pre-growth saturation times for 100g sources are frequently observed, and these increase proportionately with source dimensions. Even if the phosphorus trichloride flow is stopped during growth and then restarted, the pregrowth saturation recurs and creates a rapidly changing gas phase stoichiometry. The significance of this for the controlled growth of multilayers is that the incorporation of indigenous dopants is a strong function of the gas phase stoichiometry and consequently, rapid swings in carrier concentration have been observed in association with source saturation.[1] A typical substrate-buffer interface peak for a system using a 250g indium melt is shown in Fig. 2.1. The material grown during the uncontrolled gas phase stoichiometry demonstrates low Hall mobility (~1000 $cm^2/V\text{-}s$), suggesting a high degree of compensation. We believe the interface problem is caused by an increase in the incorporation rate for silicon and other impurities by several orders of magnitude during the changing gas phase stoichiometry associated with the source saturation sequence.

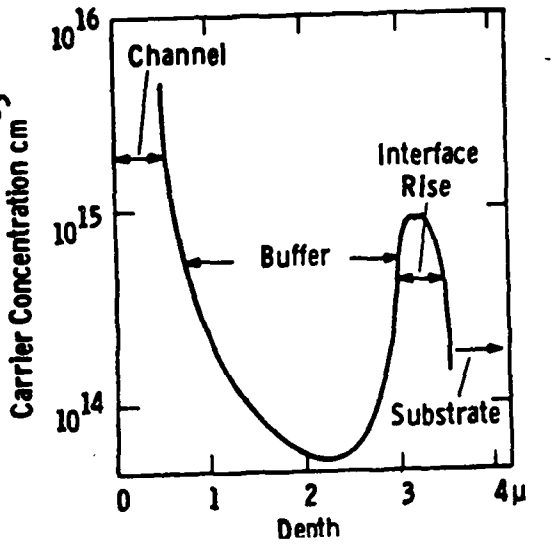

Fig. 2.1 Doping vs. depth curve illustrating enhanced impurity incorporation at epilayer substrate interface.

2.3 Gas Phase Stoichiometry-V/III Ratio

Perhaps a clearer understanding of the effect of uncontrolled gas phase stoichiometry is given by experiments in which the phosphorus and indium monochloride were added separately to the seed region of the reactor.[2] Figure 2.2 shows the dependence of the incorporation of residual dopants (probably silicon and zinc) on the V/III ratio. When the V/III ratio approached 0.33, n to p-type conversion occurred in the epitaxial layers. In a conventional reactor, the maximum V/III ratio is 0.33 (owing to the P-Cℓ ratio of 0.33) but may be less if phosphorus dissolves in the indium melt, even when the source is saturated with indium phosphide. Using mole fractions of phosphorus trichloride of 10^{-2}, low carrier concentration layers are deposited as a result of the 0.33 V/III ratio and the Mole Fraction Effect.

Silicon donors originating as silicon chlorides from a chemical attack by HCℓ on the reactor walls can be incorporated in epitaxial indium phosphide during growth depending on the HCℓ pressure over the seeds:

$$2H_2 + SiC\ell_4 \rightleftarrows \underset{\text{donor}}{[Si]} \downarrow + 4\ HC\ell\ . \qquad (2\text{-}1)$$

By mass action a dependence of the Si donor concentration on the HCℓ pressure could be expected.[3] This hypothesis explains the dependence of the residual doping of unintentionally doped indium phosphide on the phosphorus trichloride mole fraction. A mole fraction curve for indium phosphide is shown in Fig. 2.3. The carrier concentration shows a reliable dependence on the mole fraction of phosphorus trichloride provided the water vapor pressure in the reactor is low.[4]

2.4 Buffer Layers

By the use of (1) a high mole fraction of phosphorus trichloride to suppress impurity incorporation, (2) a minimal temperature gradient across the indium-indium phosphide source to provide a maximum

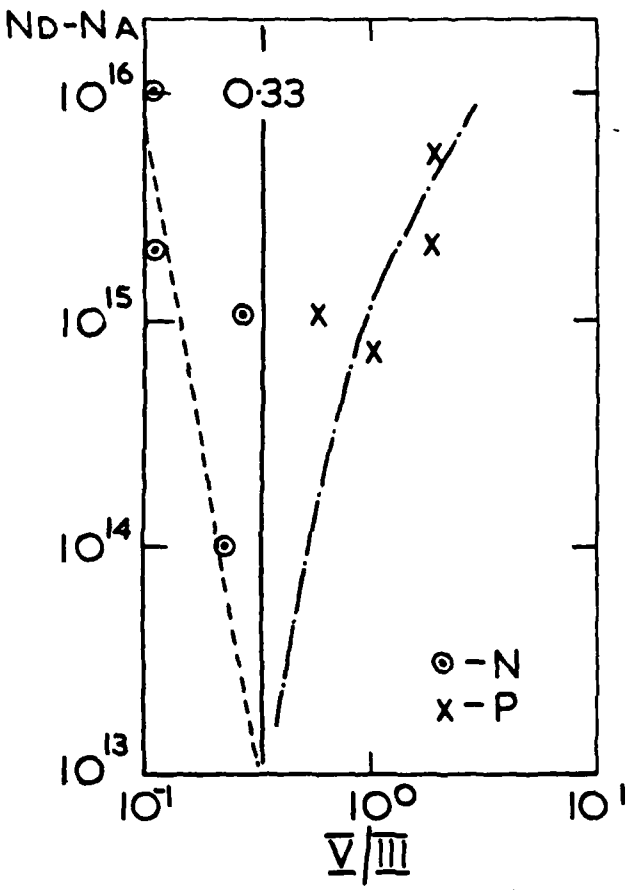

Fig. 2.2 Net impurity incorporation vs. gas phase stoichiometry, III/V ratio.

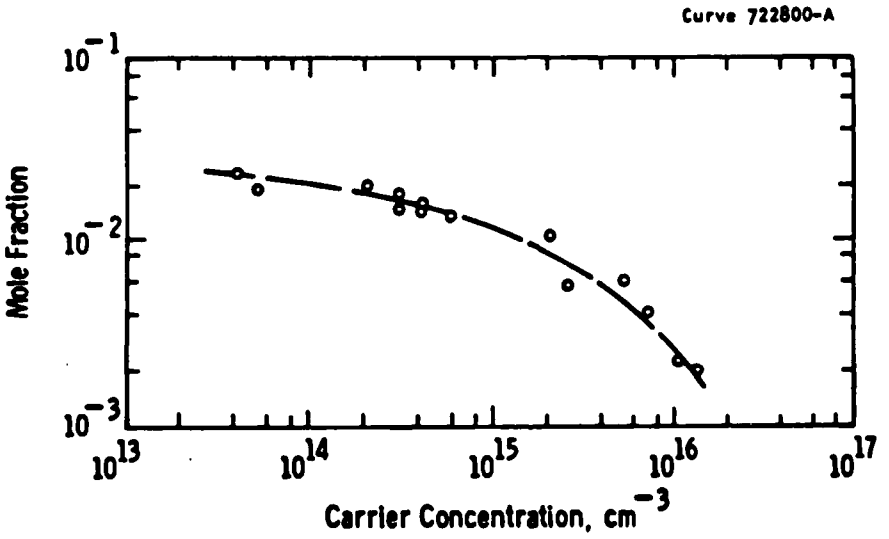

Fig. 2.3 The mole fraction of introduced $PC\ell_3$ influences the residual impurity incorporation.

V/III ratio and (3) the application of vapor phase etching to avoid the effects of source transients at the start of growth, InP buffer layers with low residual carrier concentration can be obtained. The results of Van der Pauw analysis of a series of pure buffer layers is given in Table 2.1.

Table 2.1

The Electrical Properties of Undoped Indium Phosphide Epitaxial Layers

The Van der Pauw Results of a Series of Epitaxial Layers Grown with Molar Fraction $[PC\ell_3] = 1.5 \times 10^{-2}$				
Run No.	N_D-N_A (300 K)	N_D-N_A (77 K)	μ (300 K)	μ (77 K)
88	4×10^{14}	3×10^{14}	4800	68000
89	4×10^{15}	1×10^{15}	2340	17000
90	1.6×10^{14}	3×10^{14}	3600	51000
91	9×10^{14}	7×10^{14}	3400	40000
92	6×10^{14}	3×10^{14}	3000	53000
93	3×10^{14}	2.8×10^{14}	5200	90000
94	4×10^{14}	2.8×10^{14}	4700	86000
95	2×10^{14}	1.8×10^{14}	5200	73000
96	2×10^{15}	2.1×10^{15}	3050	34000
97	2×10^{14}	1×10^{14}	5300	71000

2.5 Sulfur Doping

Most electronic devices in n-type indium phosphide require an internal structure which is usually fabricated by multilayered epitaxy. For this purpose, an impurity with predictable incorporation characteristics over a wide range of carrier concentration is added in a controlled way to the undoped buffer layers. Sulfur, which shows negligible dependence of incorporation on phosphorus trichloride mole fraction, minimum dependence on V/III ratio and is only marginally

influenced by the reactor oxygen pressure, is easily obtained as a dilute mixture of hydrogen sulfide in hydrogen. This dopant mixture is electronically monitored and diluted with hydrogen before introduction into the growth system and may be directed into the seed chamber by a minimum dead space injection valve placed adjacent to the reaction tube to reduce response time.

The growth rate of epitaxial buffer material against time is shown in Fig. 2.4 and the steady state sulfur pressure in the reactor against carrier concentration is shown in Fig. 2.5. Hence, knowing the growth rate and doping efficiency, growth schedules for multilayered epitaxy can be written. If the dopant injection circuits are small bore so as to provide minimum response time, and the injection valves and lines contain no dead space or unswept volume, it is possible to achieve rising and falling interfaces between multilayers governed by the diffusion of dopant in the semiconductor at growth temperature.

2.6 Sulfur Doped Device Structures

Figure 2.6 shows the buffer-channel interface of an FET structure. The interface width at 10^{17} cm^{-3} is 500Å, and the buffer layer carrier concentration is less than 10^{13} cm^{-3}. The buffer layer grown on the iron doped substrate is highly resistive, showing greater than 200V breakdown characteristics using tungsten probes. The channel shows a 3800-3600 cm /V-s low field mobility at 10^{17} cm^{-3} throughout its depth, suggesting that the buffer layer has successfully prevented electrical compensation by impurities from the iron doped substrate. Figure 2.7 shows the MOS profile of the FET with the mobility profile achieved by etching a Van der Pauw specimen from the same wafer.

2.7 Summary

The use of an indium liquid source with $PC\ell_3$ vapor in hydrogen to grow epitaxial InP has produced buffer ($N_D < 10^{13}$ cm^{-3}) and active layers ($N_D \approx 10^{17}$ cm^{-3}) with high mobility and good morphology. The

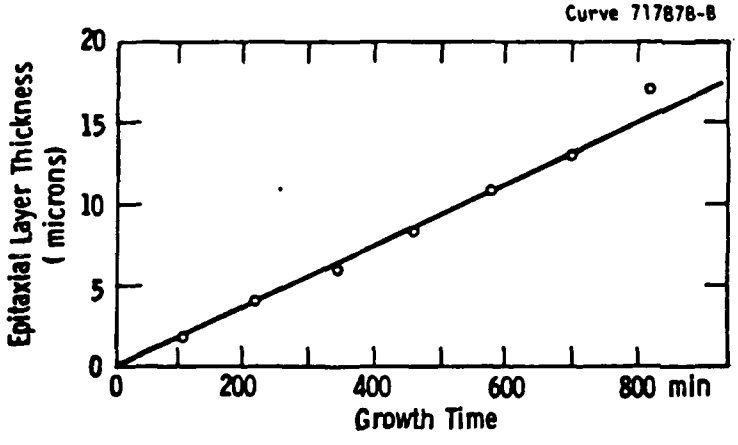

Fig. 2.4 Epitaxial layer thickness versus growth time for mole fraction $PC\ell_3 = 10^{-2}$.

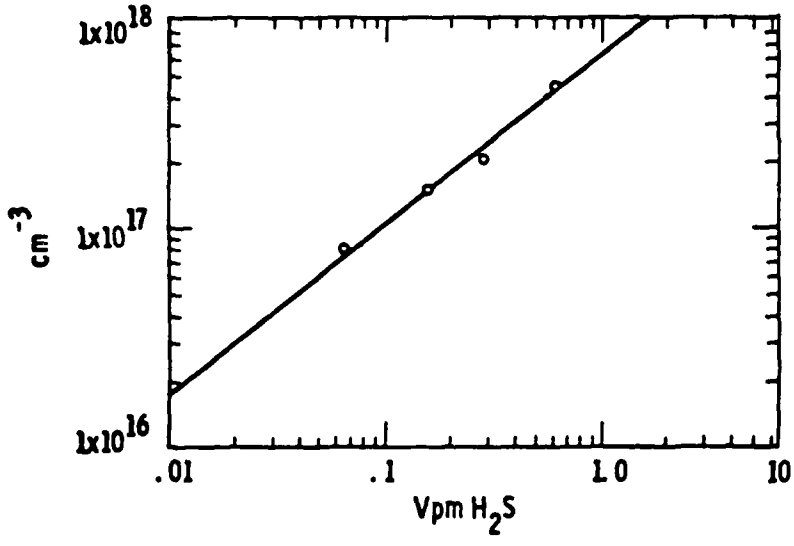

Fig. 2.5 Sulfur incorporation as electrically active impurity as a function of H_2S pressure in the reactor.

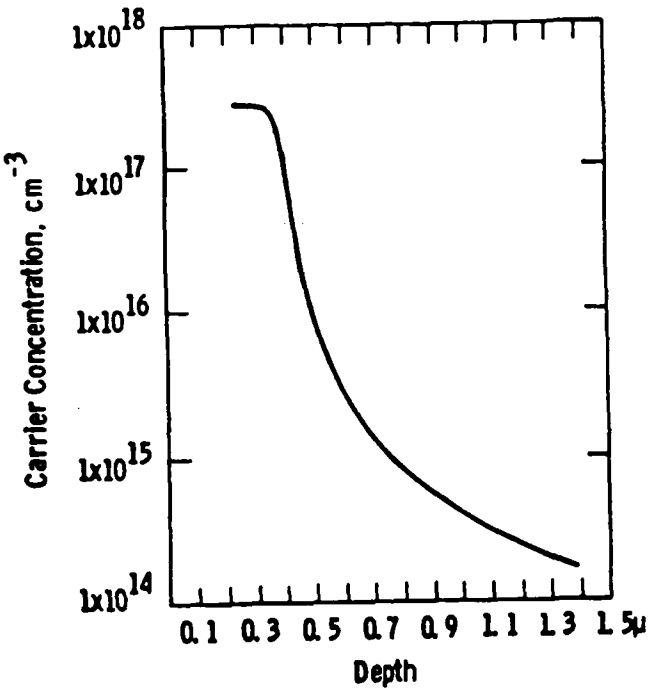

Fig. 2.6 The carrier concentration depth profile of an FET structure on a semi-insulating buffer layer.

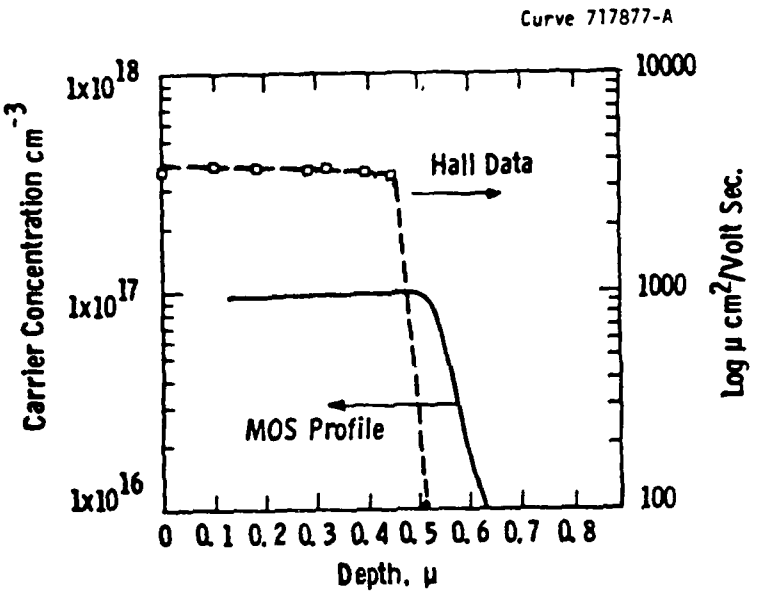

Fig. 2.7 Etching of Hall specimens shows that the surface channel mobility is retained throughout the channel.

initial problems with impurities at the buffer-substrate interface have been eliminated. However, a system that fixed the V/III ratio in the vapor over the seed crystals would offer greater stability than the present indium source method. This could well be a solid source system using $PC\ell_3$ as the transport gas which would be amenable to microprocessor sequencing for the growth of controlled device layers.

3. ION IMPLANTATION

As discussed in the previous interim report, it was concluded that a JFET would be the most suitable approach to sustain the voltages and heat associated with InP power FET operation. Therefore, it was decided that work on ion implantation should concentrate on p-type dopants with the expectation that this would ultimately be the technology of choice for the JFET fabrication.

The InP junction gate FET (JFET) requires p-type implants with (a) shallow, abrupt doping profiles typically 1000Å deep, (b) p-type doping in excess of the n-type active channel doping by at least a factor of 10, and (c) resolution of 1 micron gate lengths if selective implantation is used. P-type ion implantation in InP has been demonstrated by Westinghouse but further work is clearly required to achieve goals (a) and (b). One problem is low dopant activation, typically 20%. Mg and Be implants have profiles which obey the LSS predictions. For the high fluences which should satisfy condition (b), however, there appears to be anomalous tail diffusion and a saturation of dopant activition below the desired value.

Recent work by Tsai and Streeman[5] has given rise to a new ion implantation approach in Si (solid phase epitaxy) which has the dual benefit of high activation and abrupt electrical profiles. The objective of our study was to try and exploit similar techniques in InP p-type ion implantation. The underlying phenomena of the Tsai-Streetman work was the solid phase epitaxy of amorphous Si. By amorphizing the lattice with high dose Si implants, they provided a different host for the boron doping implants. Where the boron profile overlapped the amorphous damage profile, solid phase epitaxy at low temperatures (550°C) regrew the amorphized lattice and allowed almost complete activation, i.e. proper site location of the boron in the crystal. This

effectively truncates the tail of the LSS profile, hence satisfying both conditions (a) and (b) of our desired JFET implantation.

The same concepts should be applicable to compound semiconductors ; however, there are certain problems that need to be overcome. Oxygen has a notable effect on complexing species in both InP and GaAs, hence an oxygen-free surface must be provided before the implant and maintained through the solid regrowth step.

In addition, the implant and anneal conditions must be empirically established which predictably amorphize the crystal and provide true solid regrowth with dopant activation. The following section reviews our experimental approach to satisfying these criteria.

3.1 Experimental Results

The first criterion to satisfy in the investigation was the ability to successfully amorphize and recrystallize an InP sample. The approach was to mask one half of an InP sample with Aℓ to provide an "unimplanted" standard for comparison with the implanted half. Figure 3.1 is a schematic representation of a sample during implantation. Phorphorus was chosen as the "amorphizing" species since it increases the vacancy level on the In sub-lattice and hence aids the probable incorporation of Group II p-type dopants. Following the implant, the Aℓ was stripped from the InP using buffered HF. Rutherford backscattering data was then collected on the samples to determine the level of damage inflicted upon the InP with respect to the unimplanted reference. Following the initial backscattering measurements, annealing and another series of backscattering probes were done to determine if the damage had been successfully removed. Table 3.1 lists the series of implants performed to understand the damage-regrowth phenomenon.

Samples JC1-JC6 were the first group implanted. Figure 3.2 is representative of the Rutherford Backscattering (RBS) data collected for these samples. The backscatter data in a "random" direction is

Table 3.1

Review of Amorphization Implant Conditions

Sample No.	Fluence	Energy	Cap (Before Implant)	Sample Temp.
JC1	5×10^{14}	200 keV	---	300°K
JC3	1×10^{15}	200 keV	---	300°K
JC4	1×10^{15}	200 keV	---	300°K
JC5	1×10^{15}	200 keV	---	300°K
JC6	2×10^{15}	200 keV	---	300°K
A	1×10^{15}	200 keV	---	77°K
B	1×10^{15}	200 keV	1000Å Si_3N_4	300°K
C	1×10^{15}	200 keV	1000Å Si_3N_4	77°K
D	1×10^{15}	200 keV	---	300°K

indicative of a disordered crystal. When the data is taken on an undamaged crystal in a so-called "channeling" direction, the reflected beam is smaller than the random beam reflection. Thus, an implanted sample analyzed in a channeling direction will give a measure of the damage level relative to the two previously described extremes. We define amorphization as damage at the level of random backscatter.

Referring to Fig. 3.2, the damage from a phosphorus 5×10^{14} cm^{-2} implant essentially accomplishes amorphization of the InP lattice. Amorphization was also observed for the other samples in this series (JC3, 4, 5 and 6).

Recrystallization experiments were aimed at observing the low temperature solid phase reordering previously described for Si. By scaling the 550°C anneal temperature used in the Si work to the melting point of Si, a 400°C anneal temperature was chosen for InP. While this temperature is a significant reduction from the 700°C anneals traditionally used for low damage InP implantation, it is still enough to

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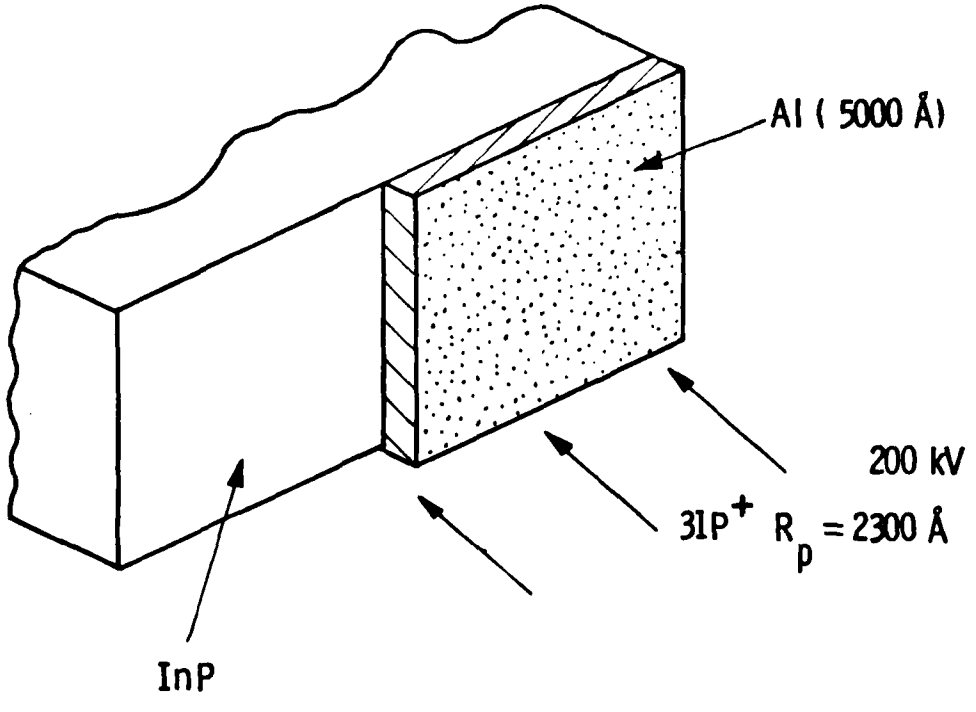


Fig. 3.1 Schematic representation of "masked" InP sample during implantation.

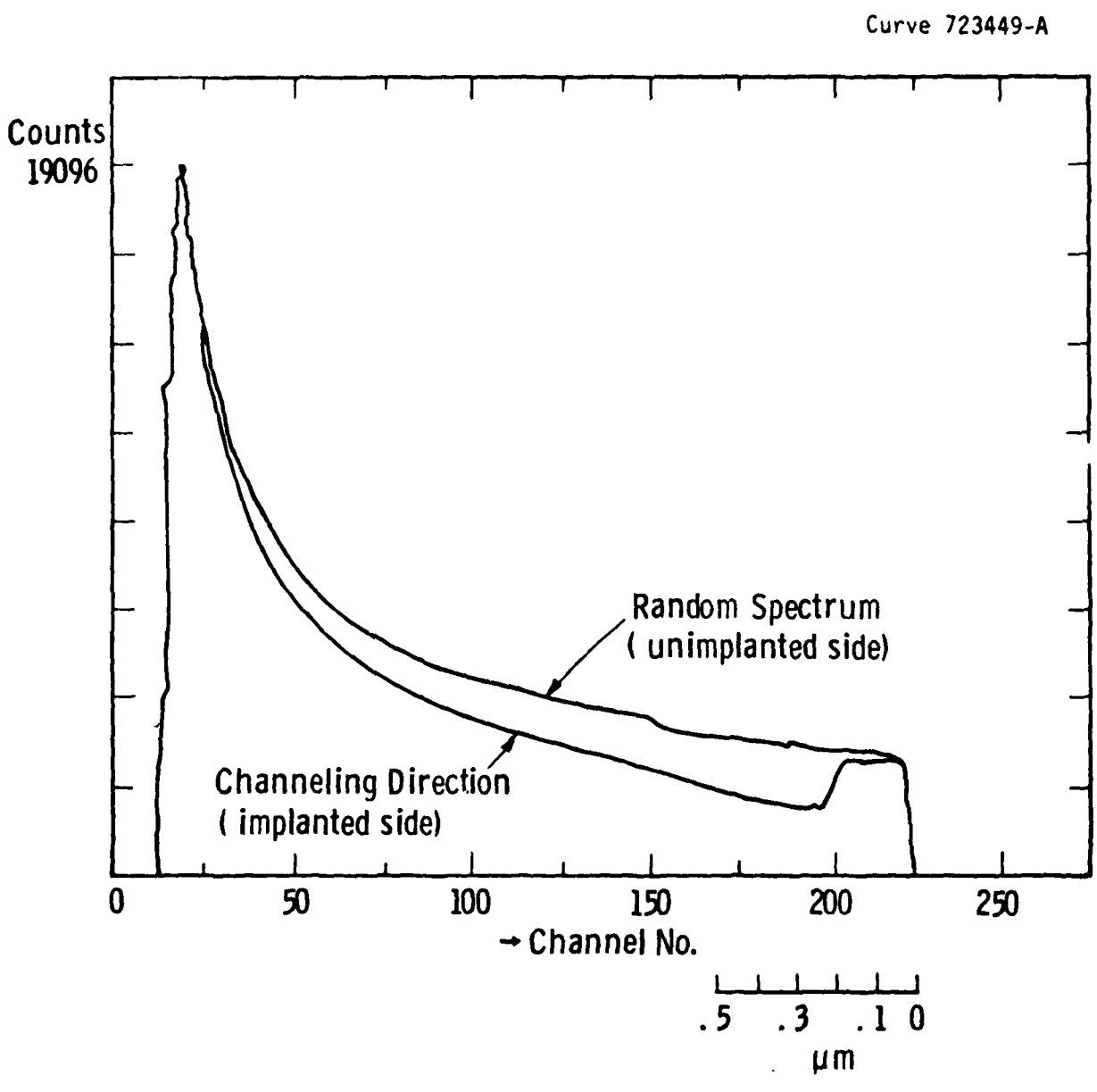


Fig. 3.2 Rutherford backscatter data for sample JC1 on both implanted and unimplanted halves.

promote thermal decomposition of the InP for the long (24 hr) times contemplated for the solid phase regrowth. Two possibilities for protecting the InP are PH_3 overpressures (capless anneals) or dielectric capping. Plasma deposited Si_3N_4 was chosen as a cap for the 400°C anneal. The Aℓ mask was stripped from the samples and deposition was performed at 340°C for 15 minutes to obtain 1000Å of Si_3N_4. This nitride is conventionally used as a cap for high temperature annealing of GaAs (860°C), and hence is of a proven quality. Twenty-four hour anneals of these samples failed to re-order the damaged region. Other workers in GaAs have observed that room temperature high dose implants have self-annealed the amorphized sample such that it does not undergo the sought after solid phase epitaxy.[6] In addition, there was some question as to the viability of capping after the implant, i.e. is there an intermediate contamination? In an effort to remove some of these questions, sample series A to D was run. The "capped" samples had Si_3N_4 over the half of the InP to be implanted, and Aℓ over the other half. A liquid nitrogen cold stage was used on samples A and C to try and minimize any self annealing during the high dose implant.

Samples B and C (implant through Si_3N_4) showed surface deterioration from the implant which prohibited further measurement. Figures 3.3 and 3.4 represent the backscatter data for A and D, respectively. The effective width of the amorphized region on sample A is larger than D. This gives a measure of the self-annealing which takes place for the 1×10^{15} implant between a liquid nitrogen temperature implanted sample (A) and a room temperature implant (D). Both samples were capped and annealed for 24 hr at 400°C as previously described. Figures 3.5 and 3.6 show the backscatter profiles for A and D, respectively, after cap, anneal and stripping of the cap. The key result from this experiment is that by minimizing the self-annealing during implantation, it becomes possible to observe the low temperature re-ordering. Sample D does show some reduction in the width of the amorphized region, but clearly sample A has had a return to crystallinity.

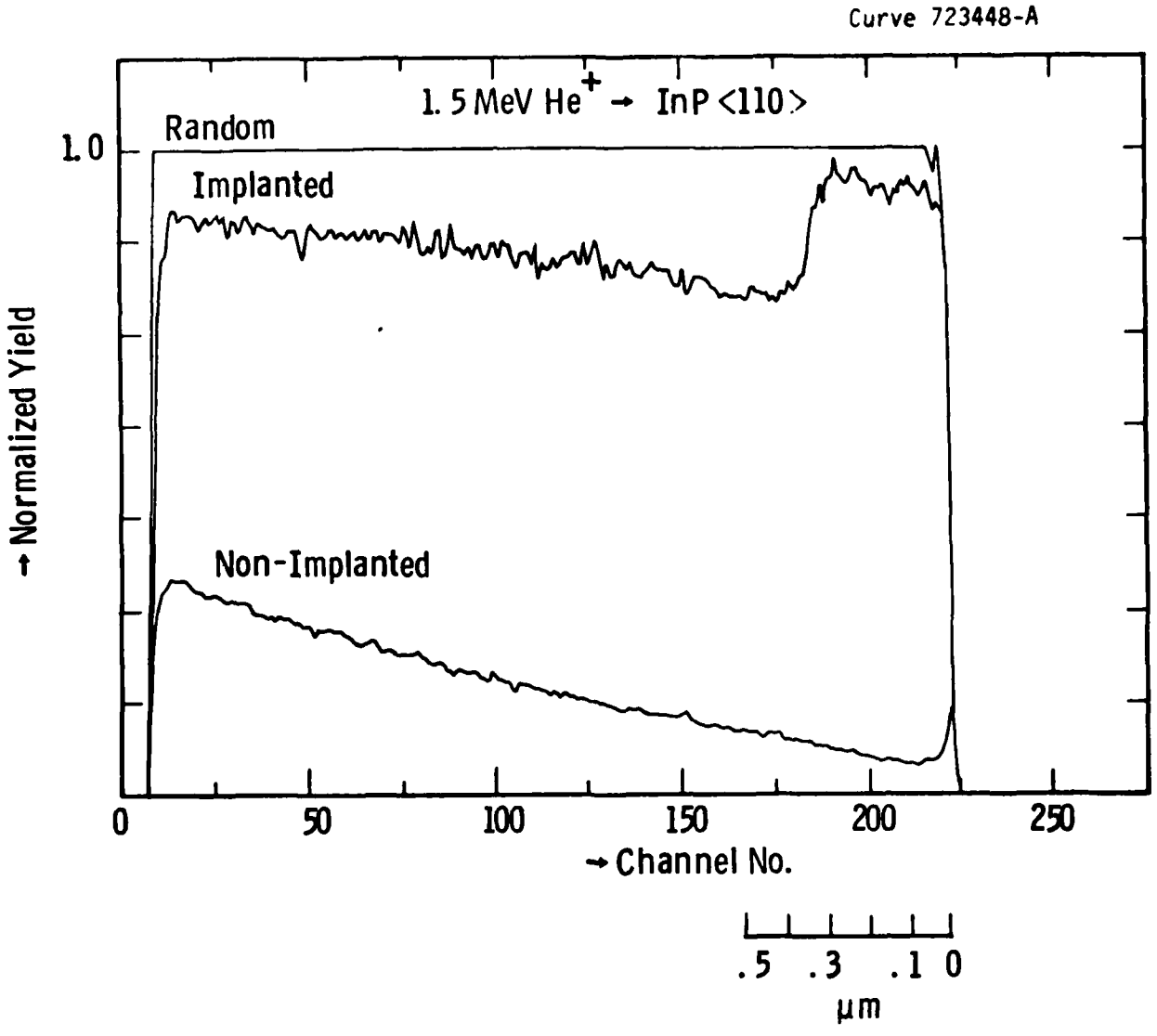


Fig. 3.3 Rutherford backscatter data for sample A before anneal.

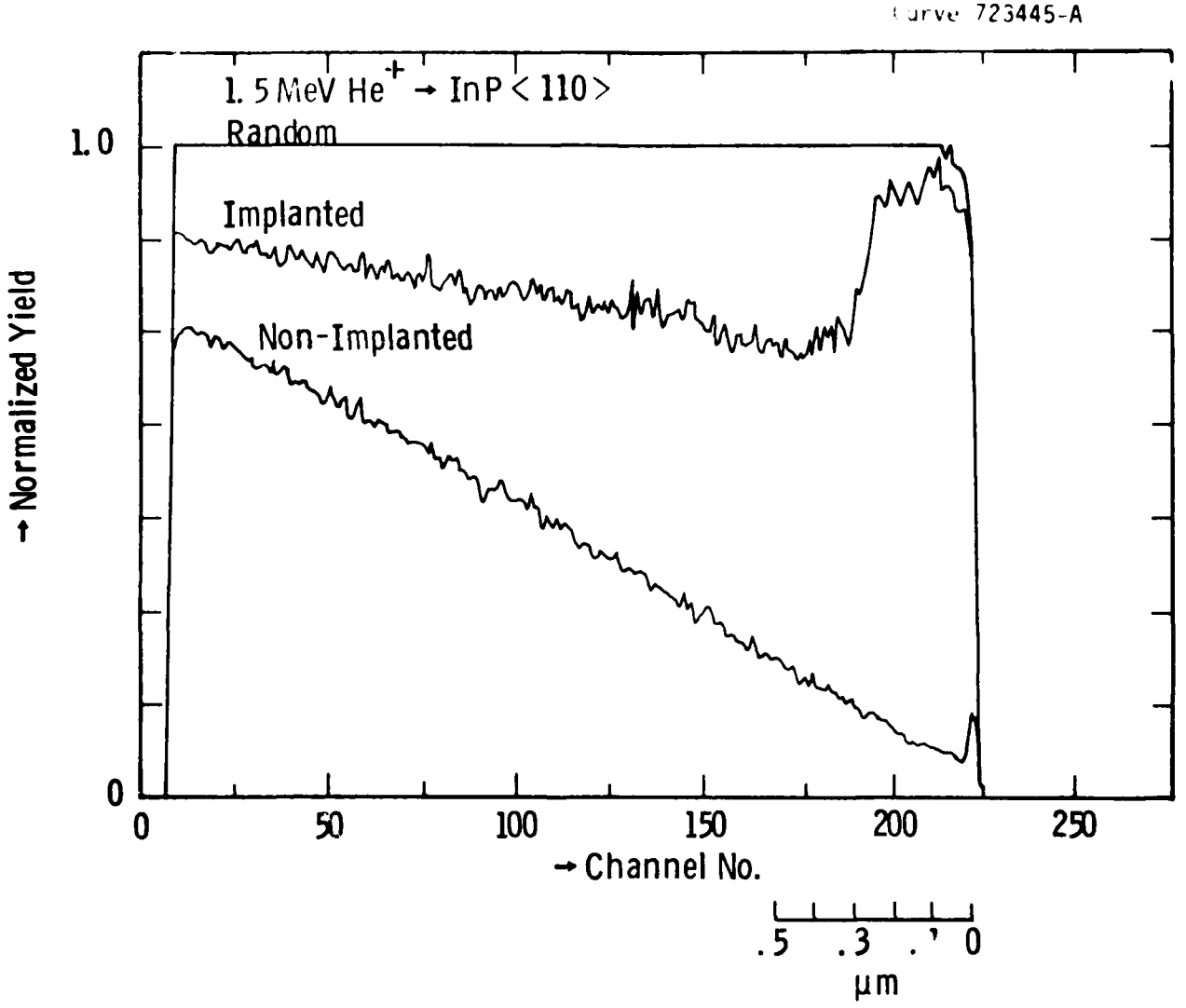


Fig. 3.4 Rutherford backscatter data for sample D, before anneal.

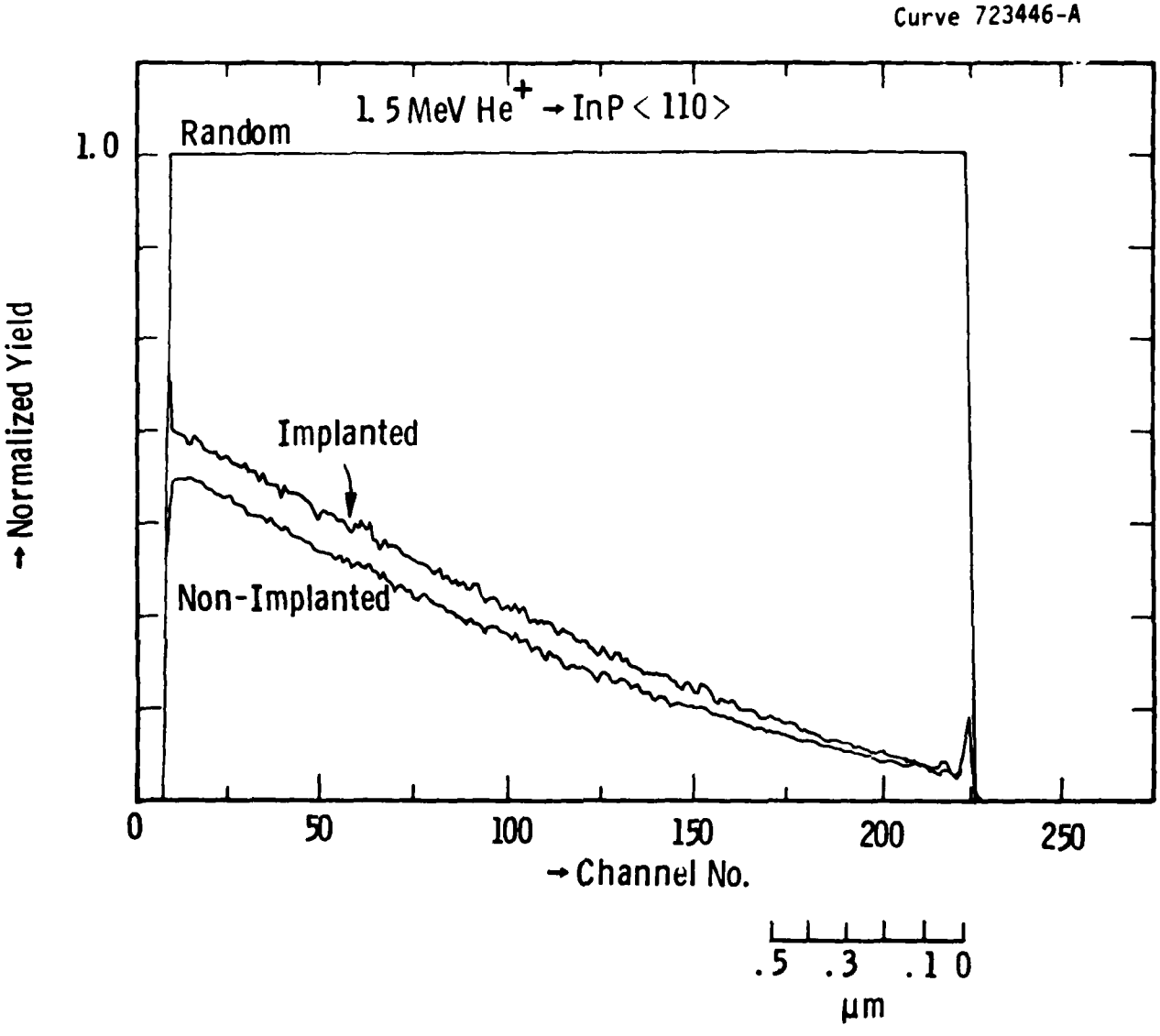


Fig. 3.5 Rutherford backscatter data for sample A after anneal at 400°C for 24 hr.

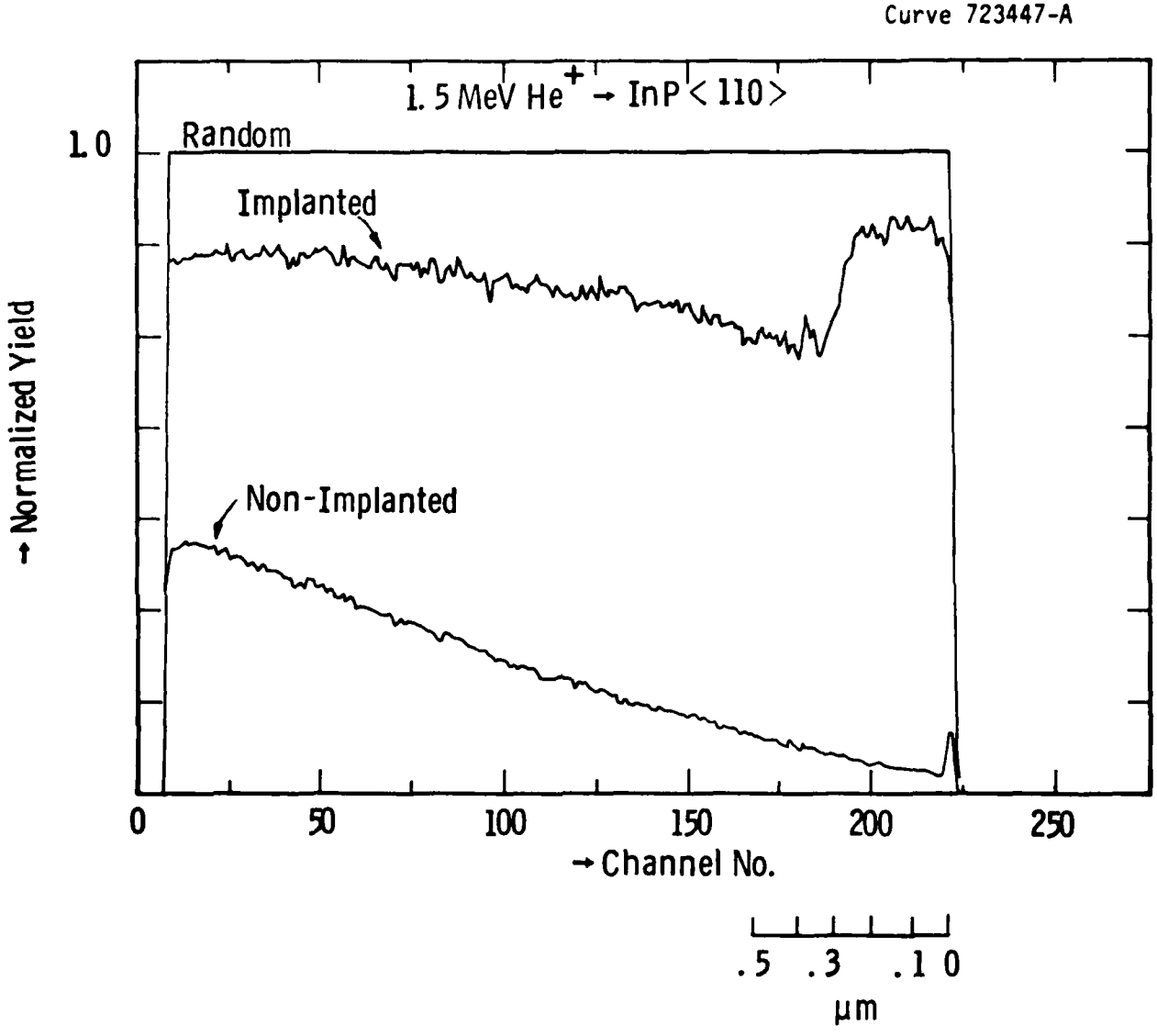


Fig. 3.6 Rutherford backscatter data for sample D after anneal at 400°C for 24 hr.

Work remains in identifying any electrical ramifications of the amorphized crystal. In particular, the initial hypothesis was that higher dopant incorporation is possible for implants of this nature. This conjecture remains to be proved. Additionally, Fig. 3.5 shows some residual damage remaining in the annealed InP. This represents possible scattering centers and hence transport degradation is a possibility. For the device of interest, it ultimately may turn out that this damage degrades the active channel of the FET. It should be pointed out that this approach extends itself to active layer preparation as well. Hence, one could envision a "deep" phosphorus damage implant followed by Si and Mg implants to create the device structure. The initial recrystallization work is encouraging and offers the possibility of a low anneal temperature implant technology for InP which obviates traditional capping failures at high temperature.

4. DEVICES

The previous section reviewed an initial study aimed at bringing ion implantation technology to bear on InP JFET Fabrication. A parallel effort was maintained to develop a diffused-junction gate technology. The following sections review the p-n junction technology, the JFET Fabrication sequence and rf performance, and concludes with a semi-quantitative comparison between comparable GaAs and InP FET's.

4.1 Diffused Junction Technology

Figure 4.1 shows the I-V characteristics of an "unassisted" Aℓ Schottky gate on n-type InP. Our previously reported work at overcoming the inherent low barrier heights on InP by using various dielectric layers between the gate and the InP was marginally successful. The desirability of a reproducible gate system ultimately weighed against the dielectric assisted barriers and in favor of p-n junctions. The idea of the diffused junction gate is to define the gate region using traditional deposition and lift techniques followed by an annealing step to produce the junction. Figure 4.2 schematically represents the steps involved in defining micron length p-n junctions. The surface metal is intended to provide an "ohmic" contact to the diffused semiconductor as well as capping the dopant species against evaporation from the sample. There should be no "phase" interference between the two elements associated with the anneal, and in addition, the surface metal should be a slow diffuser relative to the dopant. The group II elements (Mg, Cd, Zn) are the recognized choices for producing p-type doping in InP. Other workers have tried combinations like Au-Mg or Au-Zn to satisfy the aforementioned criteria. Neither choice has been successful; in the Mg-Au case the Mg tends to oxidize and hence yields non-reproducible results, while the Au-Zn system suffers from the

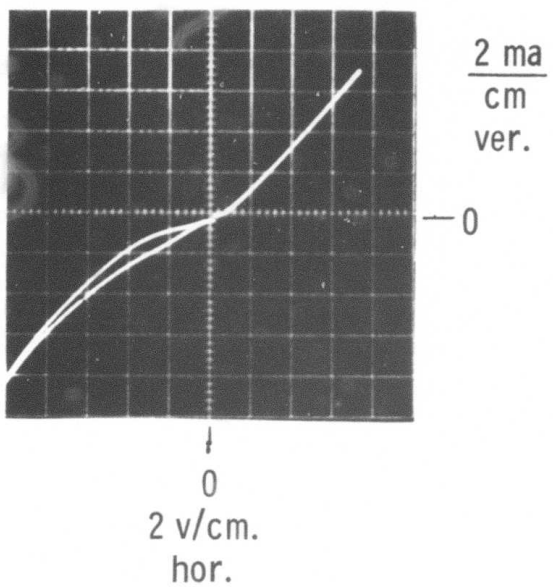


Fig. 4.1 "Unassisted" Aℓ Schottky barrier I-V characteristic on 10^{17} n-type InP.

Dwg. 7714A73

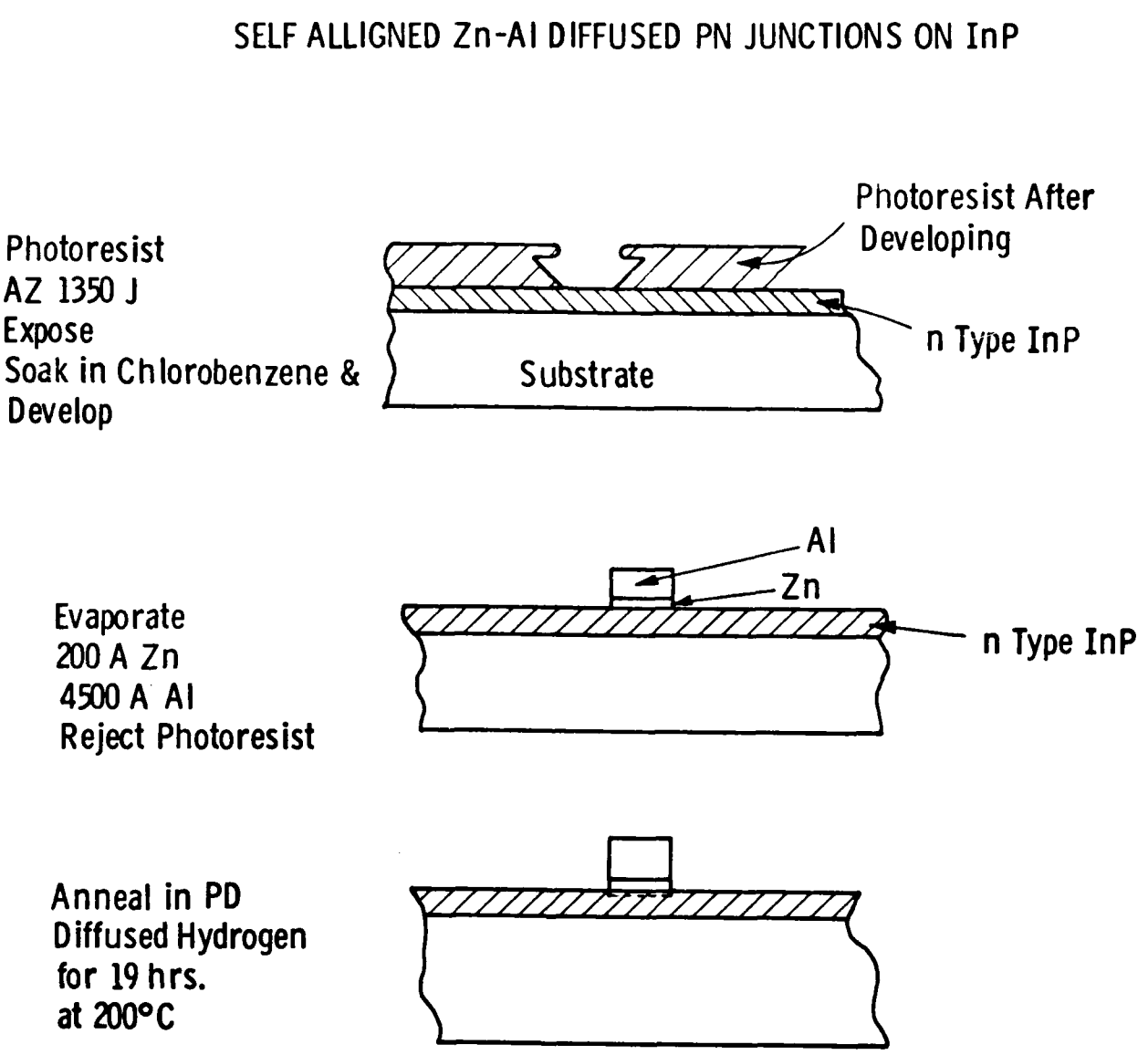


Fig. 4.2 Self aligned diffused p-n junctions on InP.

problem that the Au diffuses into the InP more rapidly than the Zn. In light of these results, an Aℓ-cap layer over Zn was tried because Aℓ is known to be a slow diffuser in III-V compounds and Zn does not oxidize as rapidly as Mg. Test samples were prepared with 200Å of Zn followed by 4000Å of Aℓ. Figure 4.3 shows an I-V characteristic of an unannealed diode with a Zn-Aℓ anode (DV-111-U). As can be seen, the device is reminiscent of a leaky Aℓ Schottky barrier on InP. Table 4.1 reviews the anneal conditions tried with the Aℓ-Zn multilayer structure. The 345°C anneal failed due to a phase transformation amongst the constituents during the heating cycle. A lower temperature, 200°C, was chosen in the belief that metallurgically the sample would stabilize and that sufficient diffusion would take place to form a p-n junction. Figures 4.4 and 4.5 represent I-V characteristics for samples DV-111-2 and DV-111-3, respectively. An improved barrier has been formed, with the longer anneal providing a larger built-in potential. Figure 4.6 is a plot of $1/C^2$ vs V for a device on sample DV-111-3. The data indicates a built-in potential of 1 electron volt, clearly superior to any reported Schottky Barrier height.

To try and determine the relative diffusion rates for Zn and Aℓ in InP at 200°C, samples DV-111-2 and DV-111-3 were subjected to in-depth profiling using sputtering Auger analysis. Figure 4.7 shows relative atomic concentrations vs sputtering time squared for both Zn and Aℓ on both samples. These plots are representative of a diffusion process. By relating sputtering time to distance (1 min = 125Å), it was possible to estimate the diffusion coefficients for Zn and Aℓ in InP held at 200°C. The results are:

$$D(A\ell)\Big|_{200°C} \sim 1.3 \times 10^{-15} \text{ cm}^2/\text{sec}$$

$$D(Zn)\Big|_{200°C} \sim 2.2 \times 10^{-15} \text{ cm}^2/\text{sec} .$$

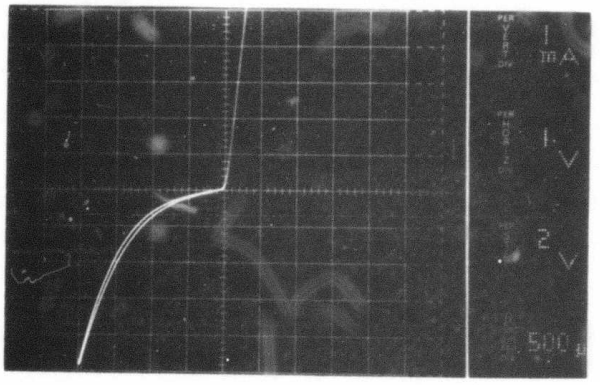


Fig. 4.3 I-V characteristic of DV111-U (5 mil test dot)

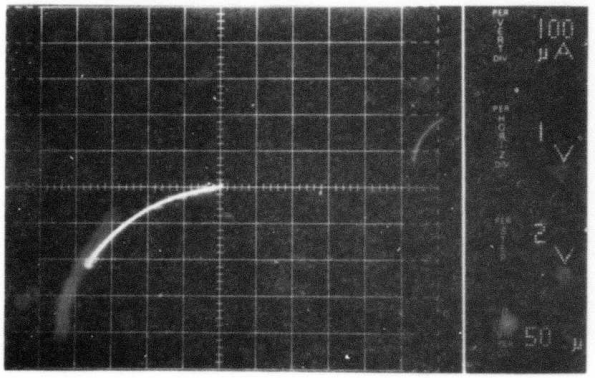


Fig. 4.4 I-V characteristic of DV111-2 (5 mil diameter test dot).

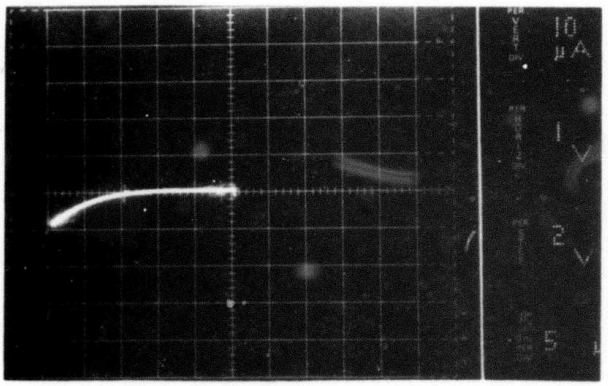


Fig. 4.5 I-V characteristic of DV111-3 (5 mil diameter test dot).

Curve 720828-A

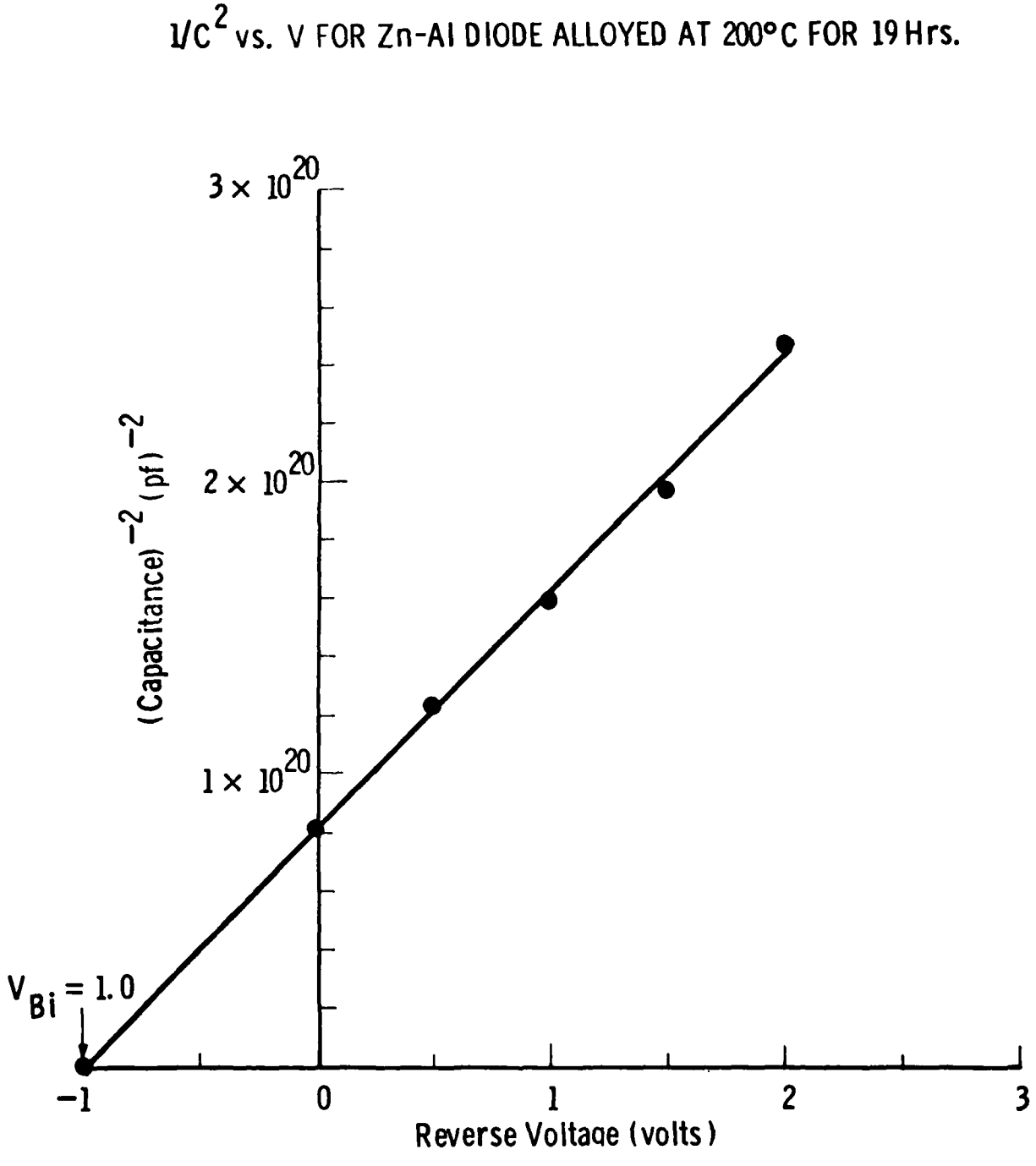


Fig. 4.6 $1/C^2$ vs V for Zn-Aℓ Diode Alloyed at 200°C for 19 hr (sample DV111-3).

Curve 722568-A

AUGER MEASUREMENTS OF AL & Zn DIFFUSION CONCENTRATION AS A FUNCTION OF DISTANCE FOR SAMPLES HELD AT 200°C for 4.5 and 19 hrs.

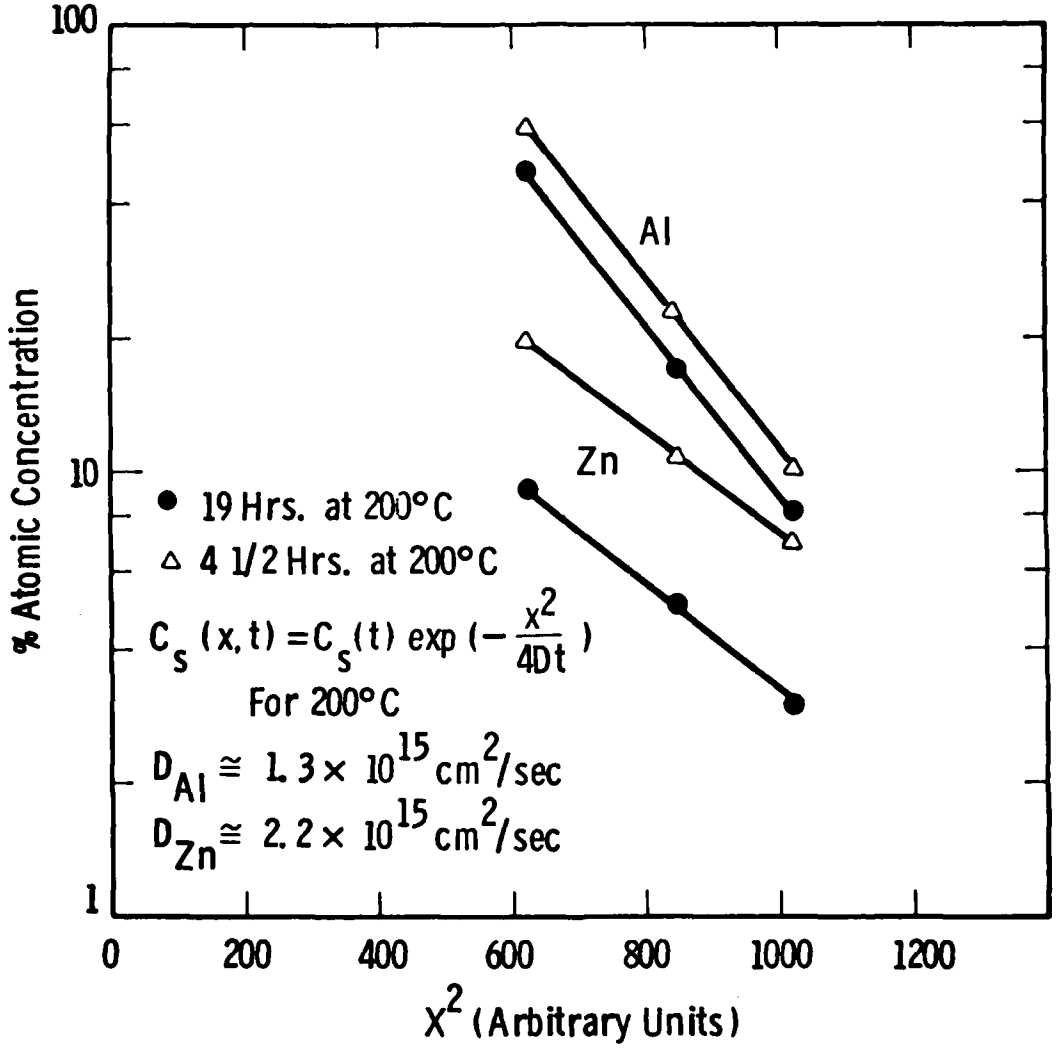


Fig. 4.7 Auger measurements of Aℓ and Zn diffusion concentration as a function of distance for samples held at 200°C for 4.5 and 19 hr.

Table 4.1

Anneal Conditions for Aℓ-Zn Diffused Junction Test Structures

Sample No.	Zn/Aℓ Thickness Å	Anneal Temp.	Anneal Time
DV-111-1	200/4000	345°C	3 min
DV-111-2	200/4000	200°C	4.5 hr
DV-111-3	200/4000	200°C	19 hr
DV-111-U	200/4000	—	—

These estimates are important for two reasons. First, they confirm the supposition that Zn will diffuse more rapidly into InP than Aℓ. More importantly, the diffusion coefficients permit a first calculation of the lateral spreading of a diffused gate device. Taking one diffusion length as a measure of the junction spreading on each side for a 19 hr anneal, one gets a figure of approximately 0.1 μm per side junction spreading. Current photolithographic limits are on the order of 1 μm geometries, hence a gate lifted off to a one micron dimension will have an electrical length of 1.2 μm for the annealing sequence just outlined. Thus, device performance comparisons between this type of JFET and a MESFET should acknowledge reasonable "scaling" parameters associated with gate lengths.

4.2 InP DJFET Fabrication and Performance

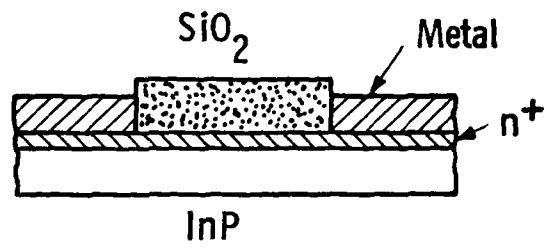
One of the attractive features of the diffused junction FET (DJFET) is that it requires only slight modification of the processing sequence for a Schottky barrier FET. Figure 4.8 is the established process sequence for an "oxide assisted" InP MESFET, and Fig. 4.9 is the modified fabrication sequence for the DJFET. Changes in the second and third mask steps represent an improvement in photoresist lifting technology and do not relate to any device design changes. The diffusion step in the DJFET process is accomplished at a low enough temperature that the ohmic contacts are left undisturbed.

Dwg. 7695A46

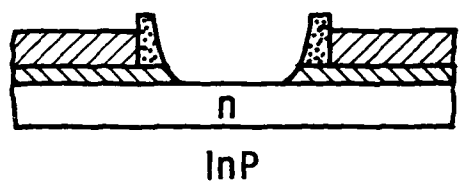
REALIGNED InP FET FABRICATION

- First Mask - Isolation
  - Photoresist - AZ111 - Expose
  - Etch InP - 1gm HIO_3 : 19cc H_2O

- Second Mask - Ohmic Contacts
  - Sputter 5000 Å SiO_2
  - Photoresist - AZ111 - Expose
  - Ion Mill + Chemical Etch SiO_2
  - Metallize and Reject
    - 600 Å Au Ge
    - 600 Å Pd
    - 3500 Å Au
  - Alloy 460°C for 15 sec



- Third Mask - Channel Thinning
  - Photoresist - AZ1350J - Expose
  - Chemical Etch SiO_2
  - Etch InP - 1gm HIO_3 : 19cc H_2O



- Fourth Mask - Gate
  - Photoresist - AZ1350J - Expose
  - Plasma Oxidize Sample
  - Cr/Au Evaporation
  - Reject Metal

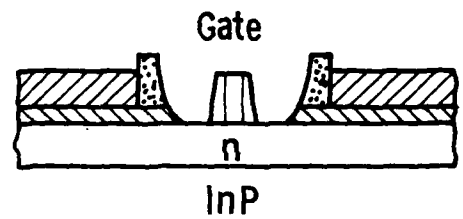


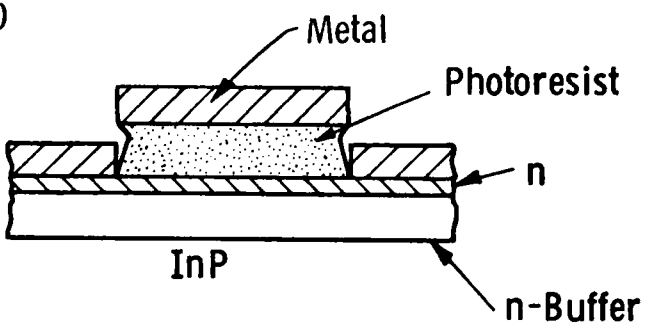
Fig. 4.8 Realigned InP FET fabrication sequence using oxide assisted gate.

Dwg. 7714A72

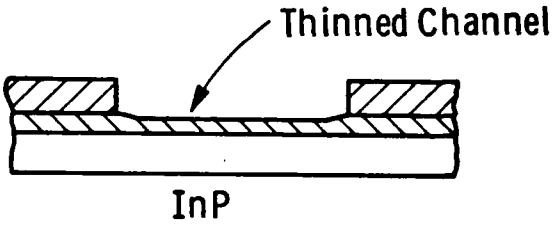
REALIGNED InP JFET FABRICATION

First Mask - Isolation
Photoresist - AZ111 - Expose
Etch InP - 1gm HIO_3: 19cc H_2O

Second Mask - Ohmic Contacts
Photoresist - AZ 1350J-Expose
Soak in Chlorobenzene &
Develop
Metallize and Reject
600 Å Au Ge
600 Å Pd
3500 Å Au
Alloy 460°C for 15 sec



Third Mask - Channel Thinning
Photoresist - AZ1350J-Expose
Etch InP-1gm HIO_3: 19cc H_2O



Fourth Mask - Gate
Photoresist - AZ1350J-Expose
Soak in Chlorobenzene &
Develop
Metallize and Reject
200 Å Zn
4500 Å Al
Anneal at 200°C for 19 hrs.

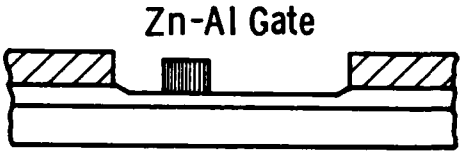


Fig. 4.9 Realigned InP DJFET fabrication.

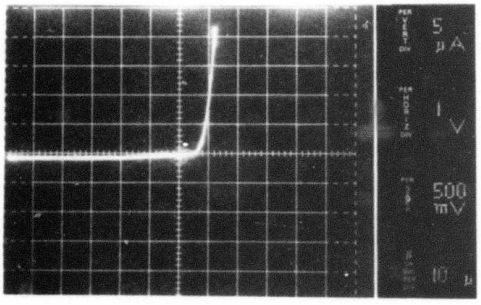
Wafers were thinned to 4 mils thickness using grit lapping, and the backside was metallized using Ti/Au/Ni/Au. The wafers were sawed, and individual devices were soldered to microwave headers using Au-Sn solder. Final wire bonding was accomplished on a heated stage thermo compression bonder. It is important to note that the device characteristics were left unchanged as a result of these final assembly steps. Because of the extremely small Zn diffusion coefficient at 200°C, it would require long term operation of the device near this temperature to effect significant channel degradation. Thus, the diffused gate device offered a reasonable vehicle for observing the potential performance of an InP JFET, both for small signal and power performance at microwave frequencies.

Figure 4.10 shows a DC I vs V characteristic of a 300 μ DJFET along with its associated gate-source performance. Figure 4.11 shows the scattering parameters measured for an InP DJFET of 300 μ periphery. Figure 4.12 is a small signal lumped element equivalent circuit for the same device. Shown in parenthesis are representative values for a similar GaAs MESFET. It should be noted that most of these lumped element values are bias sensitive.

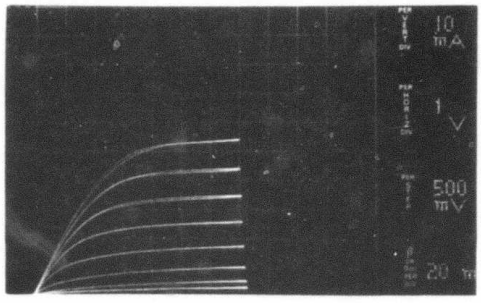
There are several interesting aspects to the equilvalent circuit of Fig. 4.12. The input resistance of both the InP and GaAs devices is on the order of 17 Ω. Also, the transconductance, g_m, and output capacitance, C_{DS}, are comparable for both devices. The major difference between the two devices is found in the gate to drain feedback capacitance, C_{gd}, and the output conductance. Both of these elements are more favorable in the GaAs FET. A more detailed discussion of C_{gd} is provided in the following section.

No two devices will be "identical." Here, for example, it can be seen that the gate-source capacitance is larger in the GaAs device than the InP device. By comparing these capacitances and the relative bias points for both devices, it was deduced that the GaAs device was doped approximately 58% higher than the InP device. Thus, it is anticipated that the higher doping would boost the gm of the GaAs

DC InP FET I-V CHARACTERISTICS



Gate-source diode properties for
1 μ × 300 μ gate



Drain characteristics for 1 μ × 300 μ
gate

Fig. 4.10 DC InP DJFET I-V characteristics.

Bias Conditions: $V_G = -2$ V $I_D = 18$ ma

$V_{DS} = 4.5$ V

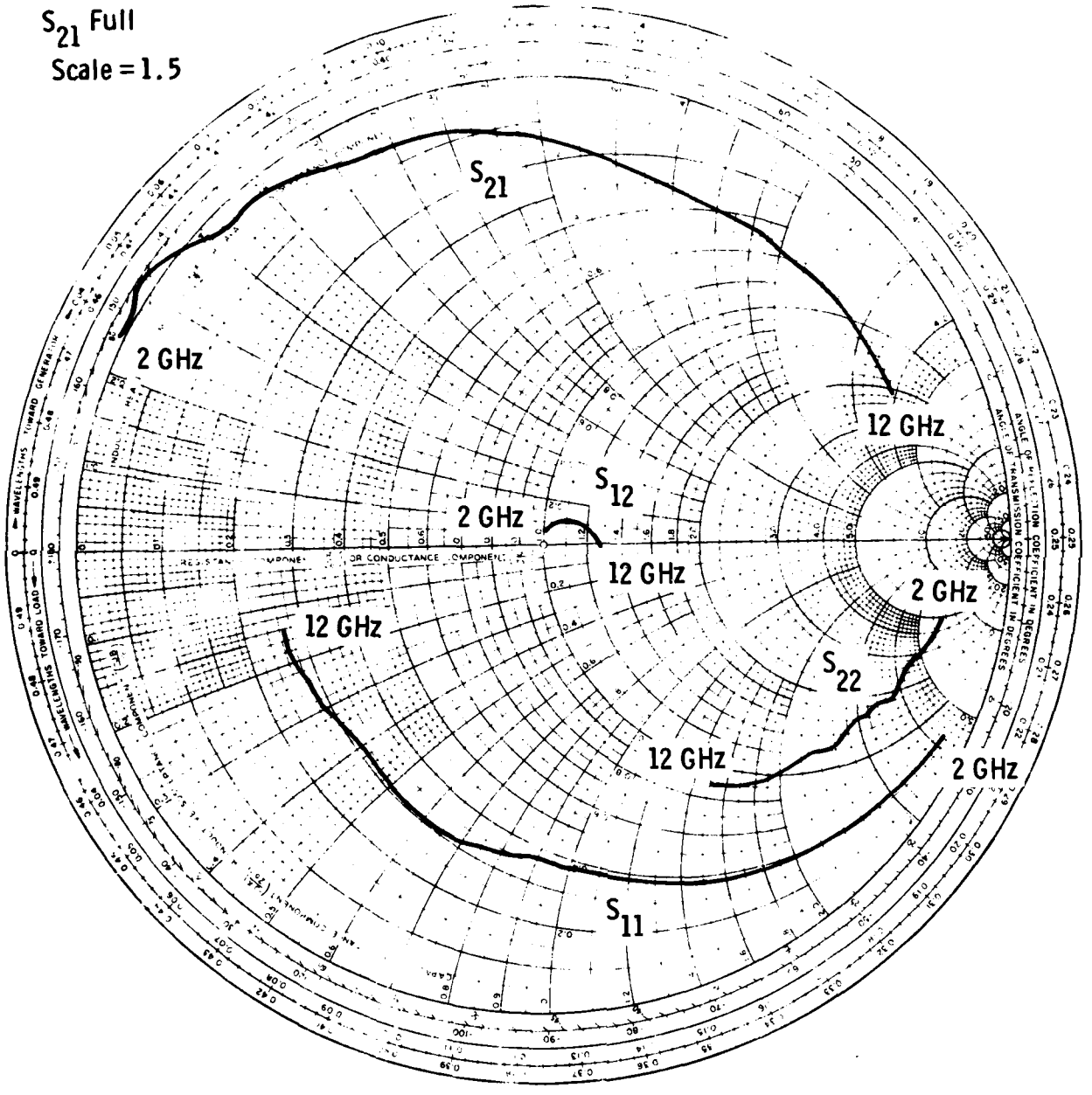
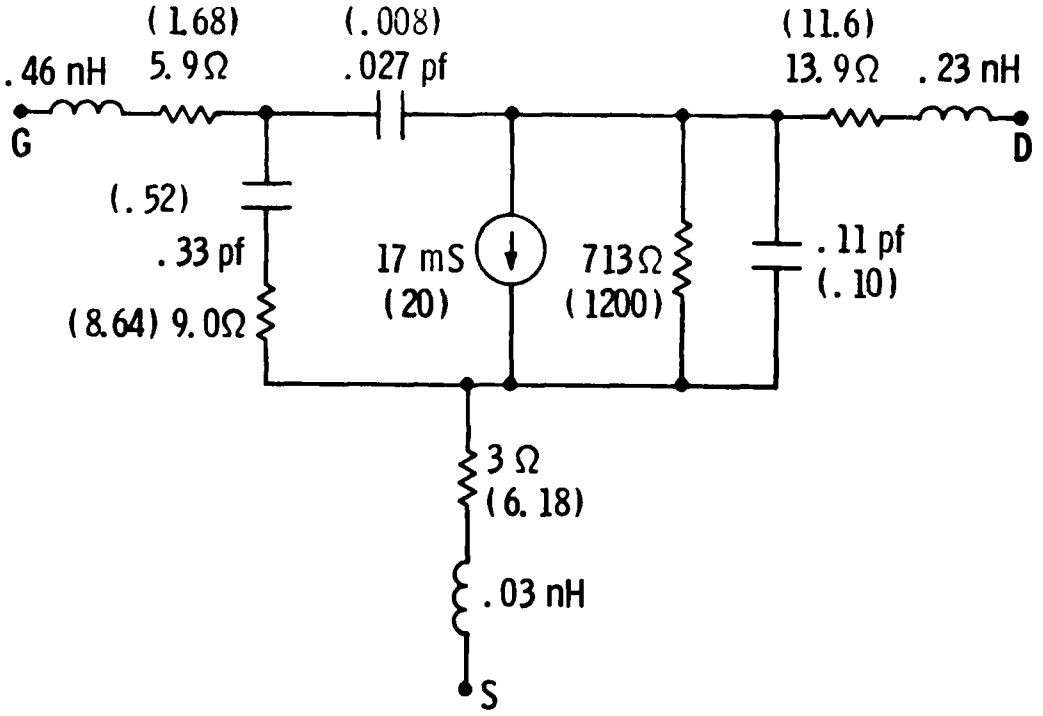


Fig. 4.11 Microwave scattering parameters for 300 μ InP DJFET measured from 2 to 12 GHz.



Frequency (6 Hz)	MAG (db) InP	MAG (db) InP (Scaled)	MAG (db) GaAs
6	11.1	–	
8	6.7	7.7	13.0
10	4.2	5.0	8.0
12	2.2	3.0	5.2

Models Valid From 2-12. Ghz
DJFET Bias: $V_G = -2V$
$V_{DS} = 4.5V$

Fig. 4.12 Broadband model of 300 μ InP DJFET. Values in parentheses are representative of a similar GaAs MESFET.

device relative to the InP device independently of material parameters. In addition, because of material differences between InP and GaAs, identical bias conditions do not necessarily reflect physically similar field geometries in two devices, hence comparisons are difficult. We shall return to this point in the next section. For now, we note that Fig. 4.12 includes scaled values for MAG which are indicative of the performance anticipated for the same device with an electrical gate length of 1μ instead of the 1.2μ length estimated for side diffusion. This scaling was done to allow a more meaningful comparison to the gain performance of the 1μ GaAs FET.

A 1200 InP DJFET was power tested at 6 GHz. Figure 4.13 shows the gain compression and power added efficiency performance of this device. Maximum output power of 200 MW with 3 dB associated gain were observed with corresponding power added efficiency of 15%. The performance of the device was primarily limited by the gain to drain breakdown of the device along with the inherently large knee voltage of the InP device. The observed knee voltage of ~4 volts for these devices implies that a large source-drain bias capability is required in order to maximize output power. Devices broke down at approximately 10.2 volts between gate and drain (gate bias at -2.5 was optimum for large signal operation); hence, the saturated power observed was reasonable vis-a-vis the device power triangle. An original motivation for looking at InP FET's was the theoretical belief that the bulk breakdown field strength of InP was larger than the value observed for GaAs. While the exact nature of gate-drain breakdown is not yet completely understood, a larger bulk breakdown strength should improve the device performance. Unfortunately, the DJFET does not clarify this issue. Current crowding leading to drain breakdown should have been inhibited by the channel recess in the device ; however, the ohmic contact technology was not completely developed and hence could be a factor. In addition, the diffused junction itself could be a source of the problem. By spreading the depletion region around the edge of the gate in the material, it is possible that the large voltage depletion zone experiences a premature breakdown similar to the case of a GaAs MESFET with an over-recessed

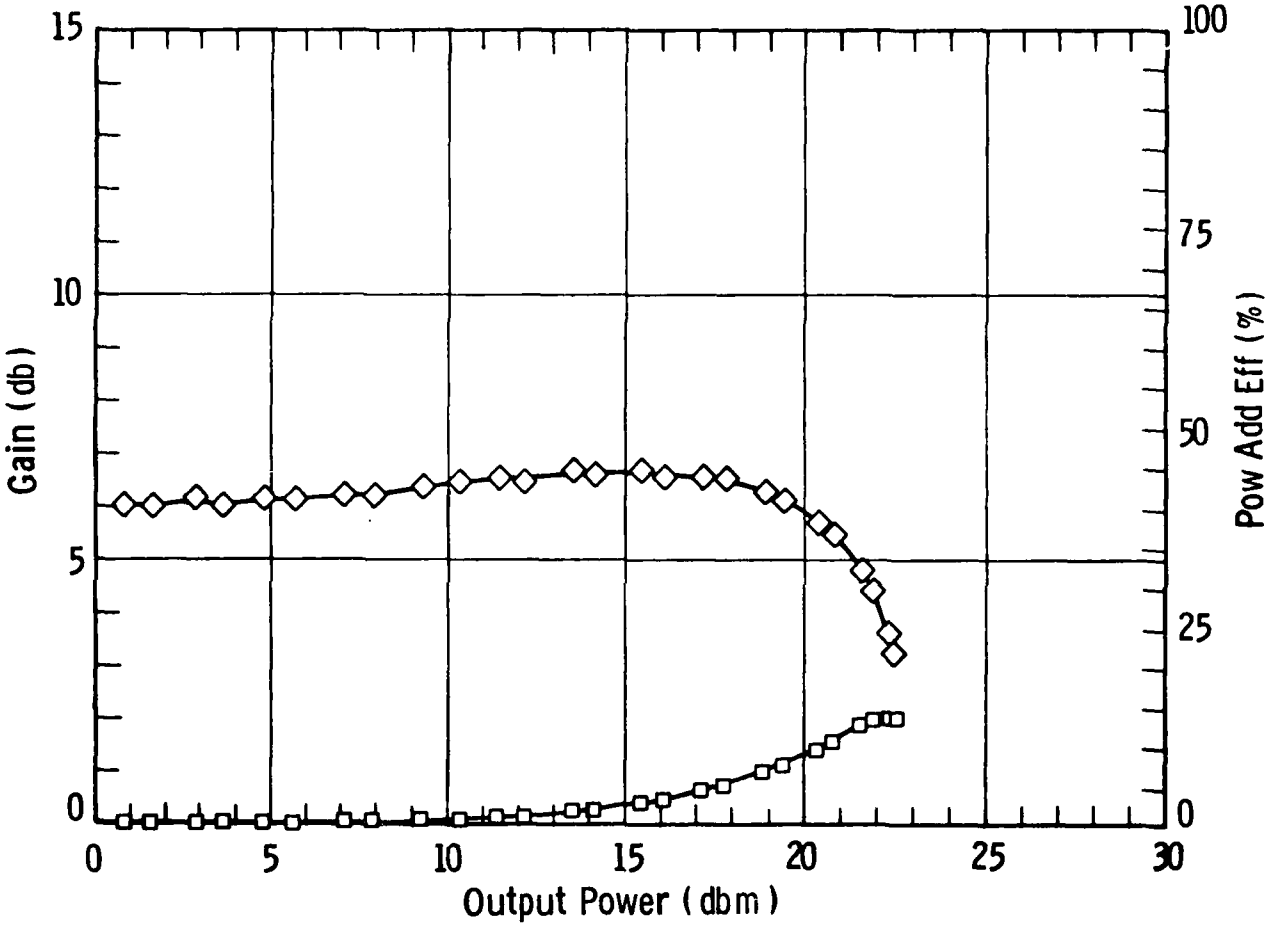


Fig. 4.13 InP DJFET (1200 μ periphery) tuned for power at 17 dbm.

gate. This problem could potentially be alleviated by going to a more sophisticated process where a uniform p-layer is created over the n-layer, and then the p-layer is removed everywhere except for the gate region. Thus, InP JFET device design requires more study to optimize the device toward its ultimate capability. Despite the non-optimum nature of the DJFET studied, it is still possible to draw some conclusions regarding the viability of InP for microwave FET applications. The following section is aimed at refining the comparison between the GaAs and InP transistors.

4.3 Comparison Between InP DJFET and GaAs MESFET

One of the key areas of controversy regarding the viability of high frequency InP FET's has been the previously observed large gate-drain feedback capacitance in InP MESFET's. The feedback between gate and drain is possible both via the active channel and the substrate. Initial hypothesis comparing the InP and GaAs devices relied upon the active channel mechanism. In particular, it was believed that strong Gunn domain formation at the drain edge of the gate in the GaAs device "de-coupled" the active channel feedback path. InP, with an acknowledged smaller negative differential mobility than GaAs, was conversely believed to have little or no domain formation in the channel, hence, C_{gd} for InP would be larger in InP than GaAs. Alternatively, if one believed that the capacitive feedback was a substrate phenomenon, a totally different conclusion could be drawn. Cr doped InP, which was used in the initial InP MESFET study, was about four orders of magnitude more conductive than its GaAs counterpart. It was therefore easy to envision a different model in which a "depletion-like" capacitive link is established between the gate-drain bus pads through the substrate. In the intervening time since the initial InP MESFET study, Fe doping of InP has led to substrates whose conductivity is close to that of Cr doped GaAs. Thus, one feedback mechanism has been removed from the problem and conceivably allows a clearer look at the issue.

The InP DJFET offers no change in feedback mechanisms from the MESFET, hence, it is valid to compare the InP DJFET C_{gd} feedback to the GaAs MESFET C_{gd} feedback.

To begin the comparison, it is important to realize the significance of C_{gd} in determining device performance. Referring to Fig. 4.12 it is clear that C_{gd} in the InP DJFET is larger by a factor of three than C_{gd} in its counterpart, the GaAs MESFET. Figure 4.14 contains three gain plots which put the importance of C_{gd} in perspective. Curve A represents the gain of the InP DJFET of Fig. 4.12 with the gate length scaled to 1μ. Curve C is the gain for the GaAs MESFET in the same figure, and Curve B is the InP DJFET of A but with its C_{gd} value of 0.027 pf replaced with the GaAs value of 0.008 pf. The DJFET performance suffers by 2 db due to the C_{gd} value at the bias point tested.

Since a large signal model can be thought of as a combination of small signal models along the power tuned load line, it is instructive to characterize the DJFET at many bias points. Figure 4.15 shows a family of curves for C_{gd} for a 300μ InP DJFET as a function of gate bias with drain bias as a parameter. In contrast, Fig. 4.16 shows a similar family of curves for a 900μ GaAs MESFET. Clearly, the behavior of C_{gd} with bias is different for the two devices. The InP DJFET has a feedback capacitance which is "depletion-like" in character, while the GaAs MESFET is opposite in nature.

No attempt at a simple relationship between the feedback capacitance and substrate conductivity was possible; however, it is clear that a fundamentally different mechanism is responsible for the feedback behavior of the InP DJFET vis-a-vis the GaAs MESFET. The averaged feedback capacitance of the InP DJFET along a "power" load line will be higher than the comparable GaAs device by a factor of three. As seen in the gain relationship shown in Fig. 4.16, this results in a sacrifice of several db of gain at X-band.

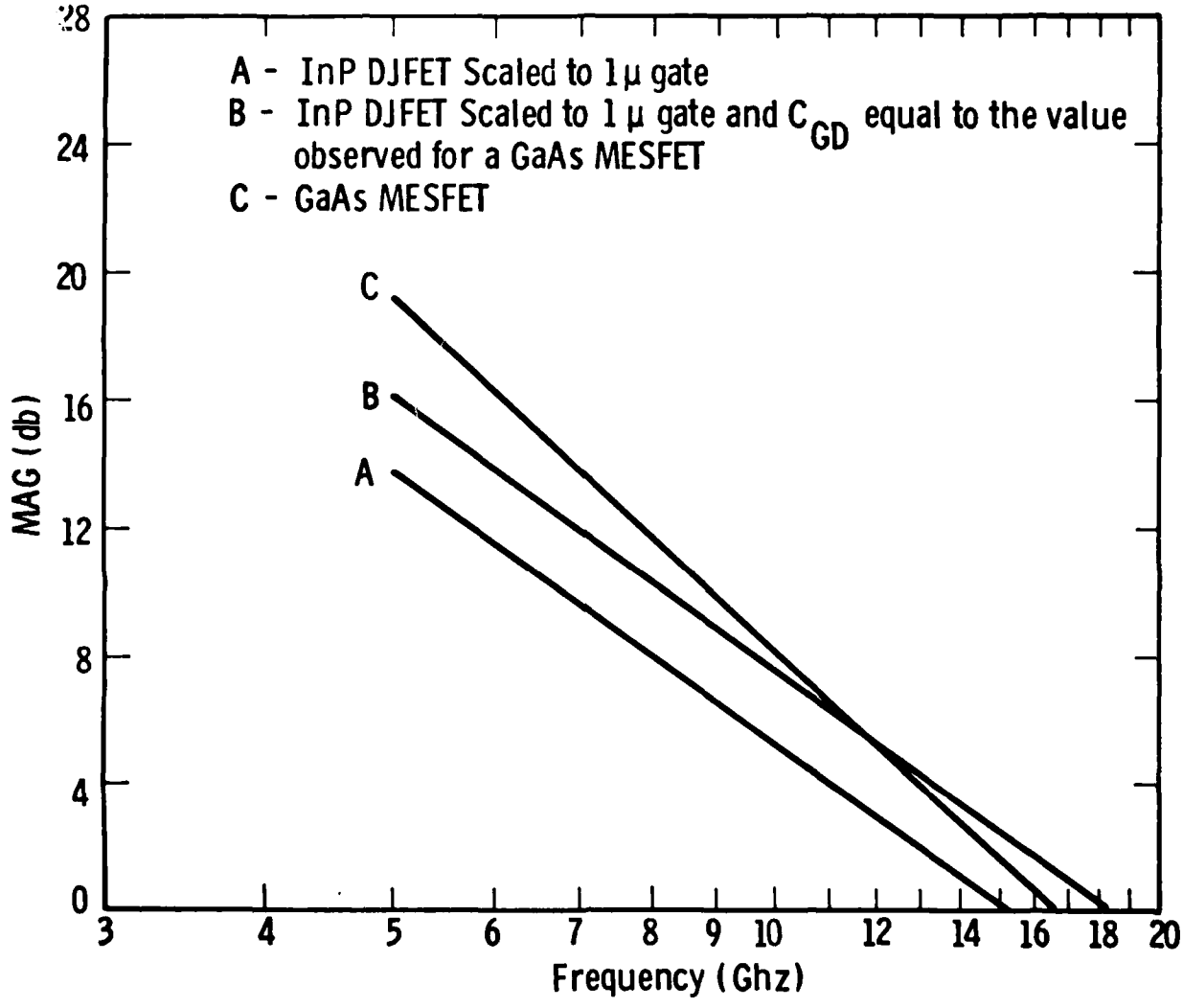


Fig. 4.14 Gain vs frequency comparison for microwave FET's.

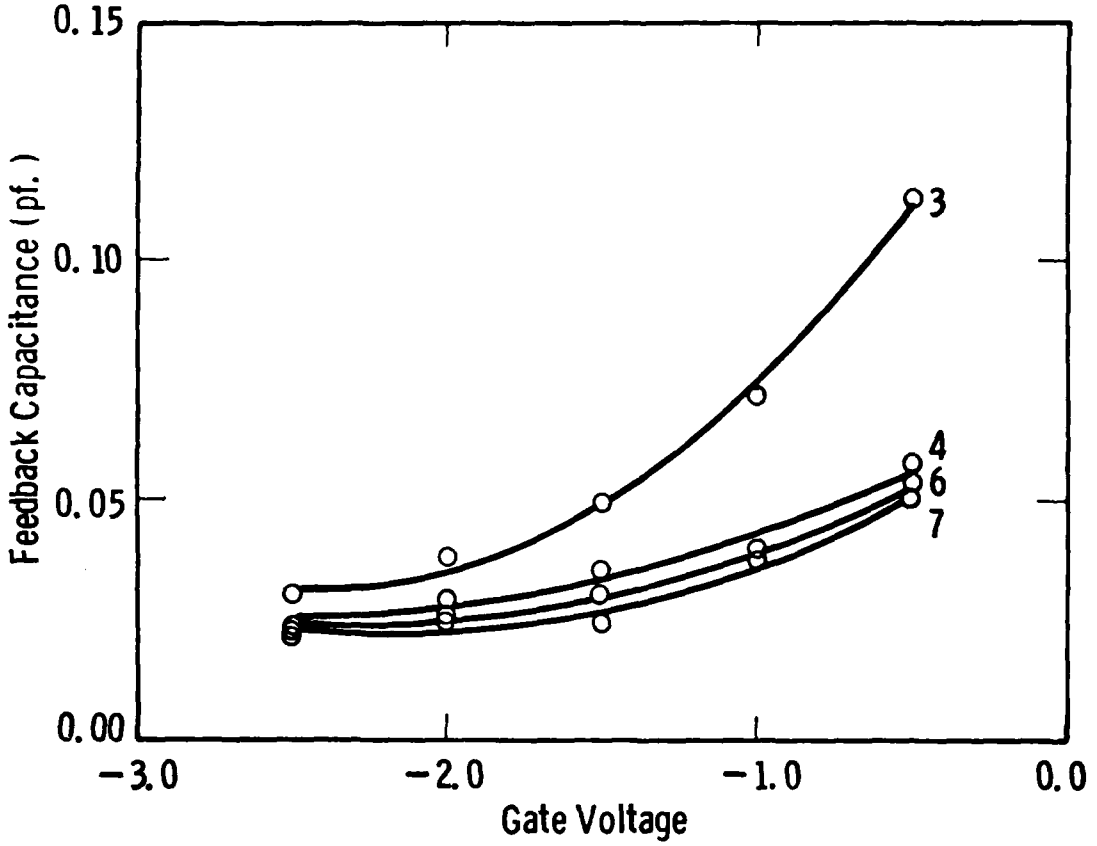


Fig. 4.15 Feedback capacitance vs gate bias w. drain bias fixed for InP DJFET (300 μ).

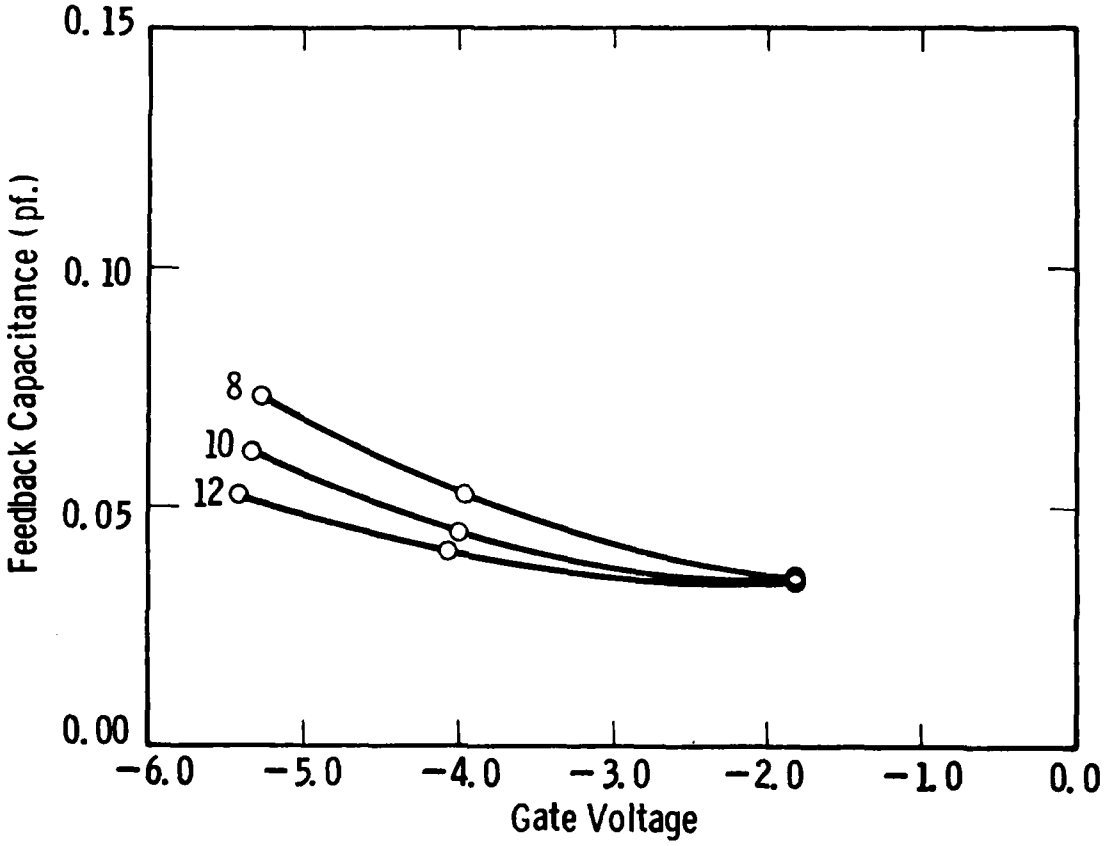


Fig. 4.16 Feedback capacitance vs gate bias w. drain bias fixed for GaAs MESFET (900 μ).

The results of the comparison between the GaAs MESFET and the InP DJFET are:

(1) Optimization and improved understanding of the InP DJFET are necessary to improve the breakdown performance of the transistor in order to allow large rf voltage swings.

(2) The inherently larger C_{gd} of InP compared to GaAs degrades the gain of the device by several db. This will be a severe disadvantage for an InP FET compared to a GaAs FET.

5. CONCLUSIONS AND RECOMMENDATIONS FOR FURTHER STUDY

As the previous chapter discussed in some detail, InP power transistors appear to suffer some deficiencies vis-a-vis their GaAs counterparts. These include the following points:

- large knee voltage
- low source-drain breakdown voltage
- large feedback capacitance.

While it is possible that further technological and device design refinements may be possible, we believe that InP microwave power transistors will present a significant challenge before they may become successful.

The work represented by this program filled in some key gaps in the InP technology. Among the achievements are:

- Well characterized, multilayer vapor phase epitaxy
- N-type ion implantation
- Amorphization and low temperature recrystallization studies
- A reproducible etching technology
- A self aligned diffused junction gate on n-type material.

Additionally, as a result of this technology development, we were able to successfully fabricate, test and analyze X-band InP JFET's. This study shows serious technical problems facing further InP power device development. Alternatively, we believe that InP technology may be usefully employed in the digital logic arena. Successful MOS device performance would allow the realization of logic gates using standard MOS layouts from silicon technology. Thus, our recommendations for further study would include:

- Reproducible ohmic contact development with specific contact resistance $\leq 10^{-6}$ Ω-cm
- Further exploitation of initial ion implantation amorphization studies - specifically directed at p-type implants
- Small signal device development and modeling at microwave frequencies to improve device design for switching applications.

Successful completion of the above tasks would undoubtedly aid the development of InP digital IC's. In addition, it should be noted that substrate development will also be required. At present, semi-insulating or n^+ InP is limited in supply and quite variable in quality. Any successful exploitation of InP will ultimately require a change in the availability of high quality material as well as further device technology development.

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8. PRESENTATIONS

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1. R. C. Clarke and W. D. Reed, "Vapor Phase Epitaxy of Indium Phosphide for FET Fabrication," Proc. of Seventh Biennial Cornell Electrical Engineering Conference, Cornell University, Ithaca, New York, August 1979.

2. V. L. Wrick, J. C. Kotvas, R. C. Clarke, and E. T. Watkins, "Self Aligned Diffused Junction InP FET's," paper presented at 1980 Workshop on Compound Semiconductors for Microwave Materials and Devices, San Francisco, February 1980.

3. V. L. Wrick, W. J. Choyke, and C.F. Tzeng, "Amorphization and Low Temperature Recrystallization of InP," paper submitted to Solid State Electronics.